Amendments to the Claims:

This listing of the claims will replace all prior versions and listings of claims in the application:

Listing of the Claims:

1-12 (Canceled)

13 (Previously Presented): A method of manufacturing an integrated semiconductor device having a plurality of semiconductor elements formed in a well region of a semiconductor layer and each having a source of a first-conductivity-type semiconductor, a drain of the first-conductivity-type semiconductor and a body region of a second-conductivity-type semiconductor between said source and said drain, and a drift layer of the first-conductivity-type in an upper region of said well region, comprising the steps of:

implanting impurities concurrently into a first drift layer of one semiconductor element and into a second drift layer of another semiconductor element, an implantation mask being used that includes a portion corresponding to said first drift layer of said one semiconductor element and having a first opening ratio as well as a portion corresponding to said second drift layer of said another semiconductor element and having a second opening ratio different from said first opening ratio, wherein

said one semiconductor element has a breakdown voltage higher than that of said another semiconductor element,

said implantation mask being used has said first opening ratio smaller than said second opening ratio, and

said one semiconductor element is adjacent to said another semiconductor element; and

providing, in said semiconductor layer, a wall-shaped element-isolation insulating film for isolating said one semiconductor element from said another semiconductor element, prior to said step of implanting impurities; and

annealing said integrated semiconductor device after said step of implanting impurities to diffuse said impurities.

14-15 (Canceled)

16 (Original): The method of manufacturing an integrated semiconductor device according to claim 13, wherein

said implantation mask has masking portions and openings in the shape of stripes, and said implantation mask is used by being placed with said stripes arranged in the direction parallel to a carrier path from the source to the drain of said semiconductor elements.

17 (Original): The method of manufacturing an integrated semiconductor device according to claim 13, wherein

said implantation mask being used is a mesh implantation mask having dot-like openings dispersed in a masking portion.

18 (Original): The method of manufacturing an integrated semiconductor device according to claim 13, wherein

said implantation mask being used is a dot implantation mask having dot-like masking portions dispersed in an opening.

19 (Canceled)

20 (Previously Presented): The method of manufacturing an integrated semiconductor device according to claim 13, wherein

an impurity concentration of said first drift layer is lower than said second drift layer.